IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Bayot	Docket No:	TI-33474
Serial No:	09/963,493	Examiner:	Coleman, William
Filed:	9/27/2001	Art Unit:	2823

For: METHODS OF AND APPARATUS FOR MANUFACTURING BALL GRID ARRAY SEMICONDUCTOR DEVICE PACKAGES

APPEAL BRIEF PURSUANT TO 1.192(c)

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on 5-21-04.

Tommie Chambers

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the Final Office Action mailed October 16, 2003.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-11 were originally filed. Claims 6-11 have been cancelled and Claims 12 - 16 have been added thus, the subject matter of the instant appeal is Claims 1-5 and 12-16.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-11. By virtue of an amendment filed on August 12, 2003, Claims 6-11 were cancelled and Claims 12-16 were added. An Amendment After Final was filed on December 13, 2003, amending no claims. The Applicants have received no Advisory Action and consequently do not know if the amendment was entered.

SUMMARY OF THE INVENTION

The present invention relates generally to the field of semiconductor device packages. Referring to Figure 1, a ball grid array semiconductor package 100 is described. Ball grid array semiconductor package 100 may comprise a substrate 103, such as an insulating substrate. For example, substrate 103 may be a film manufactured from a straight-chain non-thermoplastic polymide. Moreover, substrate 103 may have a first surface 103b, which may be a bottom portion of substrate 103, and a second surface 103a, which may be a top portion of substrate 103. Ball grid array semiconductor package 100 also may comprise a plurality of conductive bumps 107, which may be formed on conductive bump contact areas (not shown) formed on first surface 103b.

Referring to Figs. 2a-2b, an alignment apparatus 200 for manufacturing a ball grid array semiconductor package, such as a ball grid array semiconductor package 100, is described. Alignment apparatus 200 may comprise pushing means, such as a plurality of pushers 114, which may be positioned on opposite sides of a film 122, which may comprise a plurality of substrates 103.

Moreover, the pushing means may move film 122 is a predetermined direction. Alignment apparatus 200 further may include at least one means for vibrating substrate 103, such as at least one vibrator 112, which may contact at least a portion of the pushing means and also may be positioned adjacent to a first end of film 122. In one embodiment, vibrator 122 may be an ultrasonic vibrator. Alternatively, the means for vibrating substrate 103 may include a first vibrator 112, a second vibrator 112, and a third vibrator 112, which may be positioned adjacent to the first end of film 122, a second end of film 122, and a third end of film 122, respectively.

Alignment apparatus 200 further may comprise means for lifting film 122, such as at least one backup plate 116.

In operation, the pushing means may move film 122 and substrates 103 in the predetermined direction, such as towards a plurality of conductive bumps 107, which may be disposed above film 122. When substrates 103 are in an appropriate position relative to conductive bumps 107, the means for vibrating may vibrate film 122 and substrates 103. For example, when film 122 vibrates and the means for vibrating comprise first vibrator 112, second vibrator 112, and third vibrator 112 positioned adjacent to the first end of film 122, the second end of film 122, and the third end of film 122, respectively, film 122 may move in a direction towards a fourth end of film 122, for example, the end of film 122 without a vibrator 122 positioned adjacent to the end. In this embodiment, moving film 122 in a single direction may allow the conductive bump contact areas (not shown) formed on first surface 103b of substrate 103 to substantially align with a corresponding conductive bump 107. When each of the conductive bump contact areas are substantially aligned with at least one conductive bump 107, the vibration of film 122 and substrates 103 may discontinue. The means for lifting film 122 then may lift film 122 towards conductive bumps 107 disposed above film 122, such that the conductive bump contact areas may contact the corresponding conductive bump 107, which may dispose each conductive bump 107 on the corresponding conductive bump contact area.

Referring to Figure 3, a planarizing apparatus 300 is described.

Referring to Figure 4, a method 400 for manufacturing a ball grid array semiconductor package, such as a ball grid array semiconductor package 100 according to any of the described embodiments of the present invention, is described.

Referring to Figure 5, a method 500 for manufacturing a ball grid array semiconductor package, such as a ball grid array semiconductor package 100 according to any of the described embodiments of the present invention, is described.

Referring to Figure 6, a method 600 for manufacturing a ball grid array semiconductor package, such as a ball grid array semiconductor package 100 according to any of the described embodiments of the present invention, is described.

ISSUES

The two issues on appeal are first whether Claims 1 and 12 are anticipated by Chapman and second whether Claims 2-5 and 13-16 are unpatentable over Chapman in view of Kuroda.

GROUPING OF THE CLAIMS

Each of Claims 1 and 12 as contained in the attached Appendix are independently patentable and these rejected claims do not stand or fall together for the reasons more clearly set forth herein and below.

ARGUMENTS

It is respectfully submitted that Chapman does not disclose or suggest the presently claimed invention including aligning each of the conductive bump contact areas with at least one conductive bump wherein the vibration of at least one portion of the substrate substantially aligns each of the conducted bump contact areas with at least of the conductive bumps in independent Claim 1, albeit defined as a vibration of at least one of the substrate substantially aligns each of the conductive bumps area with at least one of the conductive bumps in independent Claim 12.

Chapman discloses a column 2, lines 16 different methods including vibration brushing and vacuum.

The present invention discloses vibration in a specific context namely alignment and this context is not mentioned from the above reference.

Kuroda does not cure these defects.

Kuroda does not relate to conductive bump technology and consequently could not disclose or suggest the presently claimed invention.

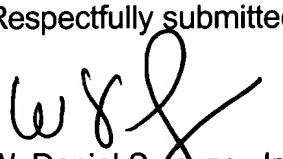
CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-6 and 12-16 under 35 U.S.C. § 102 and under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper,

including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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APPENDIX

Claim 1 (original): A method of manufacturing a ball grid array semiconductor package comprising the steps of:

providing a substrate, wherein said substrate comprises a first surface and a second surface and said first surface or said second surface comprises a conductor pattern;

providing a plurality of conductive bump contact areas on said first surface of said substrate;

substantially aligning each of said conductive bump contact areas with at least one conductive bump, wherein the step of substantially aligning said conductive bump contact areas with at least one of said conductive bumps comprises the step of vibrating at least a portion of said substrate, wherein said vibration of at least a portion of said substrate substantially aligns each of said conductive bump contact areas with at least one of said conductive bumps; and

disposing at least one of said conductor bumps on each of said conductive bump contact areas.

Claim 2 (original): The method of claim 1, wherein the step of vibrating at least a portion of said substrate comprises the step of ultrasonically vibrating at least a portion of said substrate.

Claim 3 (original): The method of claim 2, wherein the step of ultrasonically vibrating at least a portion of said substrate comprises the step of ultrasonically vibrating a first end, a second end, and a third end of a film strip on which at least one of said substrates is disposed.

Claim 4 (original): The method of claim 2, further comprising the step of discontinuing said ultrasonic vibration of at least a portion of said substrate when each of said conductive bump contact areas are substantially aligned with at least one of said conductive bumps.

Claim 5 (original): The method of claim 4, wherein said conductive bumps comprise solder.

Claims 6 - 11 (cancelled).

Claim 12 (new): A method of manufacturing a ball grid array semiconductor package comprising the steps of:

providing a substrate, wherein said substrate comprises a first surface and a second surface and said first surface or said second surface comprises a conductor pattern;

providing a plurality of conductive bump contact areas on said first surface of said substrate;

substantially aligning each of said conductive bump contact areas with at least one conductive bump, wherein the step of substantially aligning said conductive bump contact areas with at least one of said conductive bumps comprises the step of vibrating at least a portion of said substrate, wherein said vibration of at least a portion of said substrate substantially aligns each of said conductive bump contact areas with at least one of said conductive bumps;

disposing at least one of said conductor bumps on each of said conductive bump contact areas; and

reflowing said conductor bumps disposed on said conductive bump contact areas.

Claim 13 (new): The method of claim 12, wherein the step of vibrating at least a portion of said substrate comprises the step of ultrasonically vibrating at least a portion of said substrate.

Claim 14 (new): The method of claim 12, wherein the step of vibrating at least a portion of said substrate comprises the step of vibrating a first end, a second end, and a third end of a film strip on which at least one of said substrates is disposed.

Claim 15 (new): The method of claim 12, further comprising the step of discontinuing said vibration of at least a portion of said substrate when each of said conductive bump contact areas are substantially aligned with at least one of said conductive bumps.

Claim 16 (new): The method of claim 12, wherein said conductive bumps comprise solder.